Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 8-12, 14-16, 18-20, 31-33 and 44-52 are pending in the application, with claims 8, 14, 18, and 31 being the independent claims. Claims 1-7, 13, 17, 21, and 34 were previously cancelled. Claims 22-30 and 35-43 are presently sought to be cancelled without prejudice to or disclaimer of the subject matter therein. Claim 14 has been amended to correct a grammatical error. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Nonstatutory Double Patenting Rejections

The Examiner has rejected claims 8, 14, 18, 22, 26, 31, 35 and 39 under the judicially created doctrine of obviousness-type double patenting. In particular, the Examiner has rejected:

- claims 8 and 14 as being unpatentable over claim 29 of U.S. Patent No. 6,647,485 (Office Action at paragraphs 2, 3) ;
- claim 18 as being unpatentable over claim 35 of U.S. Patent No. 6,647,485 (Office Action at paragraphs 4, 5);
- claims 22 and 35 as being unpatentable over claim 1 of U.S. Patent No. 5,539,911, claim 26 of U.S. Patent No. 6,092,181 and claim 35 of U.S. Patent No. 6,256,720 (Office Action at paragraphs 6-11);

- claims 26 and 39 as being unpatentable over claim 65 of U.S. Patent No. 6,038,654 (Office Action at paragraphs 12-13); and

- claim 31 as being unpatentable over claim 29 of U.S. Patent No. 6,647,485 (Office Action at paragraphs 14-15).

By virtue of the foregoing amendment, Applicants have cancelled claims 22, 26, 35 and 39 without prejudice to or disclaimer of the subject matter recited therein, thereby rendering the rejection of these claims moot. With respect to the rejection of claims 8, 14, 18 and 31 based on obviousness-type double patenting, Applicants submit herewith a Terminal Disclaimer to Obviate a Double Patenting Rejection over (in part) cited U.S. Patent Nos. 5,539,911, 6,038,654, 6,092,181, 6,256,720, and 6,647,485.[1] Thus, the rejection of claims 8, 14, 18 and 39 based on obviousness-type double patenting are also rendered moot. Accordingly, Applicants respectfully request that the rejection of claims 8, 14, 18, 22, 26, 31, 35 and 39 based on obviousness-type double patenting be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 22-26, 28-30, 35, 37-39 and 41-43 under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,488,729 to Vegesna *et al.* ("Vegesna"). By virtue of the foregoing amendment, each of these claims has been cancelled without prejudice to or disclaimer of the subject matter recited therein, thereby

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[1] In particular, in response to a telephonic request received from the Examiner on November 30, 2004, Applicants submit herewith a Terminal Disclaimer to Obviate a Double Patenting Rejection over U.S. Patent Nos. 5,539,911, 5,689,720, 6,038,654, 6,092,181, 6,256,720 and 6,647,485, and a Terminal Disclaimer to Obviate a Provisional Double Patenting Rejection over co-pending U.S. Patent Application Nos. 10/282,045, 10/282,207, 10/283,106, 10/283,177, 10/660,671, 10/697,257 and 10/700,485.

rendering the rejection of these claims moot. Accordingly, Applicants respectfully request that the rejection of claims 22-26, 28-30, 35, 37-39 and 41-43 as anticipated by Vegesna be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

Rejection of claims 8-12, 14-16, 18-20, 31-33 and 52

The Examiner has rejected claims 8-12, 14-16, 18-20, 31-33 and 52 under 35 U.S.C. § 103(a) as being unpatentable over Vegesna in view of U.S. Patent No. 3,718,912 to Hasbrouck *et al.* ("Hasbrouck"). For the reasons set forth below, Applicants respectfully traverse.

Independent claim 8 is directed to a computer system that includes a superscalar microprocessor for processing instructions. Among other features, the recited microprocessor includes:

> a resource identifying circuit configured to concurrently identify execution resources for more than one of a plurality of buffered instructions, the identified execution resources for each of the buffered instructions including . . . a register file entry corresponding to a source of an operand for the instruction, thereby making a plurality of instructions concurrently available for execution; [and]
>
> an issue control circuit coupled to the resource identifying circuit and configured to concurrently issue more than one of a plurality of available instructions to the functional units for execution, based on availability of the execution resources identified by the resource identifying circuit and without regard to the sequential program order.

Vegesna does not teach or suggest at least the foregoing features of claim 8. In particular, Vegesna does not teach or suggest a resource identifying circuit that identifies

a "register file entry corresponding to a source of an operand" for more than one of a plurality of buffered instructions, "thereby making a plurality of instructions concurrently available for execution," and an issue control circuit that concurrently issues more than one of a plurality of the available instructions "based on the availability" of the identified register file entries.

In Vegesna, during instruction scheduling, the two instructions stored in the DBUF are tested for two types of dependencies: "intrapacket dependencies", which are defined as data dependencies that exist between the two instructions stored in the DBUF (Vegesna, col. 26, ll. 32-35), and "interpacket dependencies", which are defined as data dependencies that exist between either one (or both) of the instructions currently in DBUF and those currently in certain processor pipeline stages (Vegesna, col. 26, ll. 35-41).

If an intrapacket dependency is detected, Vegesna's instruction scheduling logic delays the issuance of the second, dependent, instruction in the DBUF for a full processor cycle to allow the first instruction from which it depends to execute. *See, e.g.*, Vegesna, col. 35, ll. 43-46, col. 37, ll. 47-56, col. 38, ll. 35-40, col. 39, ll. 12-20. The dependency is then treated as an interpacket dependency (*see, e.g.,* Vegesna, col. 35, ll. 46-52) or some other specialized processing is performed. If an interpacket dependency is detected, Vegesna's instruction scheduling logic prevents the dependent instruction from issuing until it can obtain the result of the instruction from which it depends directly from a pipeline stage for use as an input. Vegesna, col. 26, ll. 50-65. If neither dependency type is detected, the operands are accessed directly from the register file:

> If there are no interpacket dependencies, the appropriate functional unit input multiplexers (i.e. MuxC 18(c), MuxD 18(D), MuxA 20(A), MuxB 20(B), MuxStA 21 or MxStB 23) are directed by CSCHED 2 to select

> their inputs which emanate from IREGS 16; operands are accessed from the register file.

Vegesna, col. 26, ll. 50-55.

As demonstrated by the foregoing, Vegesna does not teach or suggest identifying a "register file entry corresponding to a source of an operand" for each of the instructions in the DBUF, and then concurrently issuing instructions from the DBUF "based on the availability" of the register file entries. Rather, in Vegesna, if no data dependencies are detected, the scheduler simply assumes that the necessary operand data is available in the register file and issues the instructions; if there is an intrapacket dependency, the issuance of the dependent instruction is delayed for a cycle; and if there is an interpacket dependency, the result upon which the dependent instruction depends is provided directly from the pipeline stage in which the result is generated instead of from a register file. In each case, the timing of issuance is not "based on the availability" of a "register file entry corresponding to a source of an operand" identified for each of the instructions in the DBUF.

Hasbrouck also does not teach or suggest the features of claim 8 discussed above. Significantly, Hasbrouck does not teach the recited "issue control circuit . . . configured to *concurrently issue more than one of a plurality of available instructions* to the functional units for execution" because in the instruction execution unit described in Hasbrouck, instructions can only be issued to the functional units *one at a time* via a single Execution Register 40 (*see* Hasbrouck, col. 3, ll. 58-68, and FIG. 2). Furthermore, it is unclear how the text in Hasbrouck cited by the Examiner (col. 4, lines 20-25) teaches the missing features identified above with regard to Vegesna—such as

concurrent issuance of multiple instructions based on the availability of identified register file entries.

Furthermore, even if Hasbrouck could somehow be construed as providing the missing teachings, Applicants submits that there is simply no motivation to combine the radically different architectures of Vegesna and Hasbrouck, each of which handles instruction issuance and interlocks in an entirely different manner; nor is there any teaching or suggestion of how the architecture of Vegesna could actually be modified to include the functionality described in Hasbrouck. Indeed, because Hasbrouck's instruction execution unit is limited to issuing instructions one at a time, it teaches away from a combination with Vegesna, which provides for concurrent issuance of multiple instructions.

In light of the foregoing, the combination of Vegesna and Hasbrouck cannot render claim 8 obvious. Accordingly, Applicants respectfully request that the rejection of claim 8 under 35 U.S.C. § 103(a) be reconsidered and withdrawn. Claims 9-12 and 52 are also not rendered obvious by this combination for the same reasons as independent claim 8 from which they depend and further in view of their own respective features. Accordingly, Applicants likewise respectfully request that the rejection of claims 9-12 and 52 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Like claim 8, independent claims 14, 18, and 31 also include the feature of concurrent issuance of multiple instructions based on the availability of identified register file entries. As described above, this feature is neither taught nor suggested by the combination of Vegesna and Hasbrouck, and thus the rejection of claims 14, 18 and 31 under 35 U.S.C. § 103(a) should be reconsidered and withdrawn. Claims 15, 16, 19, 20, 32 and 33 are also not rendered obvious by this combination for the same reasons as

independent claims 14, 18 and 31 from which they depend and further in view of their own respective features. Accordingly, Applicants likewise respectfully request that the rejection of claims 15, 16, 19, 20, 32 and 33 under 35 U.S.C. § 103(a) be reconsidered and withdrawn.

Rejection of claims 27, 36 and 40

The Examiner has rejected claims 27, 36 and 40 under 35 U.S.C. § 103(a) as being unpatentable over Vegesna in view of U.S. Patent No. 5,142,633 to Murray *et al.* ("Murray"). By virtue of the foregoing amendment, each of these claims has been cancelled without prejudice to or disclaimer of the subject matter recited therein, thereby rendering the rejection of these claims moot. Accordingly, Applicants respectfully request that the rejection of claims 27, 36 and 40 as obvious over Vegesna in view of Murray be reconsidered and withdrawn.

Rejection of claims 44, 46, 48 and 50

The Examiner has rejected claims 44, 46, 48 and 50 under 35 U.S.C. § 103(a) as being unpatentable over Vegesna in view of Hasbrouck as applied to claim 8 and further in view of Murray. Claims 44, 46, 48 and 50 depend from independent claims 8, 14, 18 and 31, respectively. As set forth above, claims 8, 14, 18 and 31 are not rendered obvious by the combination of Vegesna and Hasbrouck, since the combination does not teach or suggest concurrent issuance of multiple instructions based on the availability of identified register file entries as recited in those claims. Murray does not provide this

missing teaching and thus the combination of Vegesna, Hasbrouck and Murray cannot render obvious claims 8, 14, 18 and 31. Consequently, claims 44, 46, 48 and 50 are also not rendered obvious by the combination of Vegesna, Hasbrouck and Murray for the same reasons as independent claims 8, 14, 18 and 31 from which they depend and further in view of their own respective features.

Claim Objections

The Examiner has objected to claims 45, 47, 49 and 51 as being dependent upon a rejected base claim. By virtue of the foregoing remarks, Applicants have traversed the rejection of the claims upon which claims 45, 47, 49 and 51 depend. Accordingly, Applicants respectfully request that the Examiner's objection to claims 45, 47, 49 and 51 be reconsidered and withdrawn.

Other Matters

Applicants note that a Sixth Supplemental Information Disclosure Statement was filed in the present application on October 20, 2004 pursuant to 37 C.F.R. § 1.97(b). Applicants respectfully request that the Examiner initial and return a copy of the Form PTO-1449 enclosed with the Sixth Supplemental Information Disclosure Statement, and indicate in the official file wrapper of this patent application that the documents have been considered.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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